REMARKS

Claims 1-26 were pending. Claims 1-3, 5-8, 11, 14, 19, and 24 have been amended for clarification purposes. Therefore, claims 1-26 remain pending subsequent entry of the present amendment.

In the present Office Action, claims 1-9, 11-17 & 19-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,801,208 ("Keshava"), in view of U.S. Patent No. 6,819,321 ("Hsieh"), and in further view of U.S. Patent No. 6,825,848 ("Fu"). In addition, claims 10, 18 & 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Keshava, in view of Hsieh, and in further view of Fu, and still in further view of U.S. Patent No. 6,681,297 ("Chauvel").

Applicant respectfully traverses the above rejections and requests reconsideration in view of the following discussion.

Applicant's presently claimed invention recites a number of features which are distinctly different than any of those disclosed by the cited art. For example, Applicant's claimed invention generally recites a method and apparatus which concerning the cacheability of graphics data responsive to whether and how often particular data is considered during the rendering of an image. Such an approach and features are distinctly different from, and wholly absent from, the cited art.

For example, claim 1 recites an apparatus which includes a graphics unit configured to:

> "partition images to be rendered into a plurality of subset areas;
> track the number of times data corresponding to each of the subset areas is considered during the rendering of a first image; and
> determine for each of the subset areas whether data corresponding to a subset area is cacheable." (emphasis added).

In the present Office Action, Fu is cited as disclosing the above highlighted features in the following excerpts:

> "Yet another embodiment of the present invention is a method of performing graphics processing where the first cache flags comprise a plurality of first reference counters and a plurality of first age status stacks. The second cache flags comprise a plurality of second reference counters and a plurality of second age status stacks.
>
> Yet another embodiment of the present invention is a method of performing graphics processing where availability of the graphics data in the first and second caches are ascertained. Texel coordinates are received. First and second tag addresses are ascertained from the texel coordinates. The first tag addresses are compared with first content identities of the first cache lines belonging to the associated one of the plurality of first sets of the associated one of the plurality of slots. Based on the results of the comparisons, a first graphics data available status or a first graphics data not available status is returned. The second tag addresses are compared with second content identities of the second cache lines belonging to the associated one of the plurality of second sets. Based on the results of the comparisons, a second graphics data available status or a second graphics data not available status is returned.
>
> Yet another embodiment of the present invention is a method of performing graphics processing where first cache flags are updated based on availability of the graphics data in the first and second caches. First and second age statuses become youngest when updated based on the availability of the graphics data in the first and second caches. The first and second reference counters are reset or incremented based on the availability of the graphics data in the first and second caches. Oldest first and second cache lines are selected and updated to be youngest depending on the availability of the graphics data in the first and second caches.
>
> Yet another embodiment of the present invention is a graphics processing system comprising a first cache, a second cache, an engine and a frame buffer. The first and second caches contain a plurality of first and second cache lines. The first cache is partitioned into a plurality of slots. The first cache receives data from a system memory. The second cache receives the data from the first cache. The first cache and the second caches are synchronized with each other.
>
> Yet another embodiment of the present invention is a graphics processing system comprising an age status tracking means, first and second reference counters and first and second internal counters. The age status tracking means keep track of a least recently used second cache line and a least recently used first cache line. First and second reference counters keep track of how many times data in the

> respective first and second cache lines have been requested. The first and second internal counters keep track of how many times requested data in the respective first and second cache lines have been transferred. The least recently used first and second cache lines are selected to be overwritten with data to be received." (Fu, col. 2, line 30 – col. 3, line 19).

However, Applicant submits Fu does not disclose the above highlighted features. It is first noted that Fu makes absolutely no reference to tracking the number of times data corresponding to each of the subset areas is considered during the rendering of a first image. Keeping track of the age of a cache line, and how many times data in the cache line have been requested, are distinctly different concepts from tracking the number of times particular data is considered during the rendering of a first image. Generally speaking, Fu discloses a method for preventing overwriting of an L2 cache line which has been requested, but not yet transferred. For example, Fu teaches:

> "The L2 internal counters are tracked by another process (not shown). The L2 reference counter tracks the number of times a content of an associated L2 cache line is requested, i.e., if a data transfer is requested from an L2 cache line to an L1 cache line, a respective L2 reference counter would be incremented by 1. The L2 internal counter tracks the number of times a content of an associated L2 cache line is transferred.
>
> Prior to overwriting an L2 cache line, the L2 reference counter and the L2 internal counter are compared. If the L2 reference counter contains a higher value, there is data in the L2 cache line which have been requested but not yet transferred. In that case, the overwriting process is stopped until the L2 internal counter matches the L2 reference counter, i.e., the requested data is in fact transferred. This ensures that an L2 cache line is not overwritten with new data before the old data is transferred to the L1 cache.
>
> . . .
>
> Similar to the L2 cache, the L1 internal counters are tracked by another process. The L1 reference counters and the L1 internal counters ensure that data in selected L1 cache lines which have been requested but not yet transferred to the engine are not overwritten." (Fu, col. 12, line 49 – col. 13, line 37).

As can be seen, Fu does not disclose tracking the number of times particular data is considered during the rendering of a first image. Further, Fu generally does not discuss the rendering process at all.

In addition, it is believed the above makes it clear that Fu does not disclose determining for each of the subset areas whether data corresponding to a subset area is cacheable. The concept of data being cacheable or non-cacheable is wholly absent from Fu.

In view of the above, Applicant submits each of the independent claims recite features neither disclosed nor suggested by the cited art, either singly or in combination. Therefore, each of claims 1, 11, and 19 are patentably distinguishable from the cited art and a prima facie case of obviousness has not been established.

In addition to the above, while each of the dependent claims are believed patentable for at least the reasons given above, additional features are cited by the dependent claims which are not disclosed or suggested by the cited art. For example, each of claim 2-4 recite features concerning the number of times particular data is considered during the rendering of a give image. There is nothing in the cited art which discloses tracking the number of times particular data is considered during the rendering of a give image. Generally speaking, Fu is cited as disclosing these features. However, as already discussed above, the counters and flags of Fu disclose an entirely different method and mechanism. In addition, the resetting prior to a new rendering, and the incrementing responsive to considering data, as recited in claim 5 are not disclosed by Fu.

Further, claim 6 recites that data evicted from the graphics unit cache is stored in the shared cache only if the indicator indicates the evicted data is cacheable. Keshava is cited as disclosing (without any particular references) the features of claim 6. However, Keshava merely discloses an allocation mechanism which determines whether a cache may or may not be shared. However, Keshava does not disclose evicted data may or may not be cached in the shared cache responsive to an indication which indicates whether the evicted data is cacheable.

Applicant believes the application is in condition for allowance. However, should the examiner believe issues remain which would prevent the application from proceeding to allowance, the below signed representative would appreciate a phone interview at (512) 853-886 in order to facilitate a more rapid resolution.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-98000/RDR.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,

Rory D. Rankin
Reg. No. 47,884
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin,
Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: April 22, 2005